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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

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Applicant(s): Adrian Stoica

LIST OF PRIOR ART CITED BY APPLICANT
(Use several sheets if necessary)

Filing Date: January 29, 2002

Group: 2133

				U. S. PATENTS				•
Initials	Patent No	. Issue Date	Name			Class	Subclass	Filing Date
CVL	5,677,691	10-14-0797	HOSTICKA ET AL.			341	155	06-25-93
CVL	5,705,938	01-06-98	KEAN			326	39	09-05-95
CAL	5,959,871	09-28-99	PIERZCHALA ET AL.			364	489	12-22-94
CVL	5,970,487	10-19-99	SHACKLEFORD ET AL.			707	6	08-13-97
CVL	6,360,191	03-19-02	KOZA ET AL.			703	6	01-05-99
CVL	6,363,517	03-26-02	LEVI ET AL.			716	16	06-17-99
CVL	6,378,122	04-23-02	LEVI ET AL.			716	16	06-17-99
	· · · · · · · · · · · · · · · · · · ·	FOI	EIG	N PATENT DOCUME	NTS			<u> </u>
Initials	Document Number	Date		Country	Name			Translation? (Yes/No/n/a)
Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)							
CVL	Layzell, P., "A New Research Tool for Intrinsic Hardware Evolution", 1998, Second International							

NASA/ DoD Workshop

Stoica, Adrian, "Toward Evolvable Hardware Chips: Experiments with a Programmable Transistor Array," April 1999, Proceedings of the Seventh International Conference

Stoica, A., Keymeulen, D., Salazar-Lazaro, C., Hayworth, K., and Tawel, Raoul, "Toward On-board Synthesis and Adaption of Electronic Functions: An Evolvable Hardware Approach," March 1999, IEEE, Vol. 2, pp. 351-357

Conference ICES98, pp. 47-56

Perkowski, M., Chebotarev, A., and Mishchenko, A., "Evolvable Hardware or Learning Hardware?

Induction of State Machines from Temporal Logic Constraints," July 1999, Proceedings of the First

Stoica, A., Keymeulen, D., Tawel, R., Salazar-Lazaro, C., and Li, W., "Evolutionary experiments with a fine-grained reconfigurable architecture for analog and digital CMOS circuits," July 1999,

Proceedings of the First NASA/DoD Workshop,

Stoica, A., Klimeck, G., Salazar-Lazaro, C., Keymeulen, D., and Thakoor, A., "Evolutionary Design of Electronic Devices and Circuits," July 1999, IEEE, Vol. 3, pp. 1271-1278

Examiner's Signature:

CVL

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Date Considered:

9/9/05

Initial if reference was considered, whether or not citation with MPEP. Mark through citation if not considered. Include a copy of this citation form with your next correspondence to the Applicant(s).

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